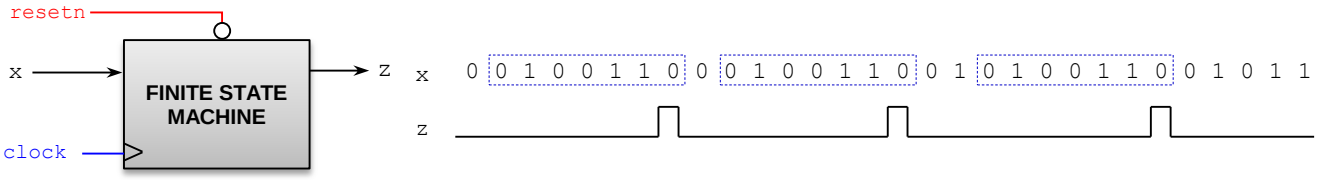
Solutions - Homework 4

(Due date: March 29th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (23 PTS)

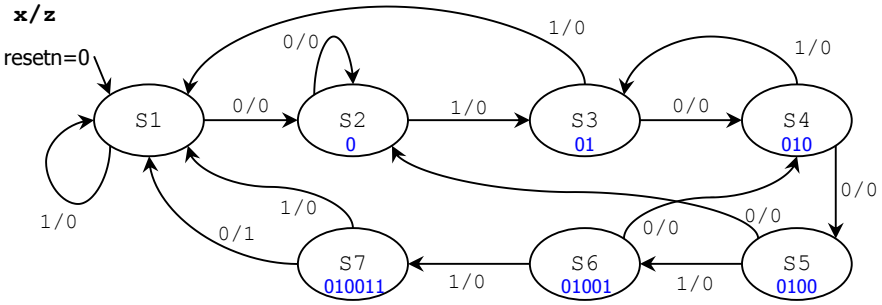
- Sequence Detector: The machine has to generate z=1 when it detects the sequence 0100110. Once the sequence is detected, the circuit looks for a new sequence.



- Draw the State Diagram (any representation), State Table, and Excitation Table. Is this a Mealy or a Moore machine? Why?
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

- *State Diagram, State Table, and Excitation Table*:

State Assignment:
S1: Q=000
S2: Q=001
S3: Q=010
S4: Q=011
S5: Q=100
S6: Q=101
S7: Q=110



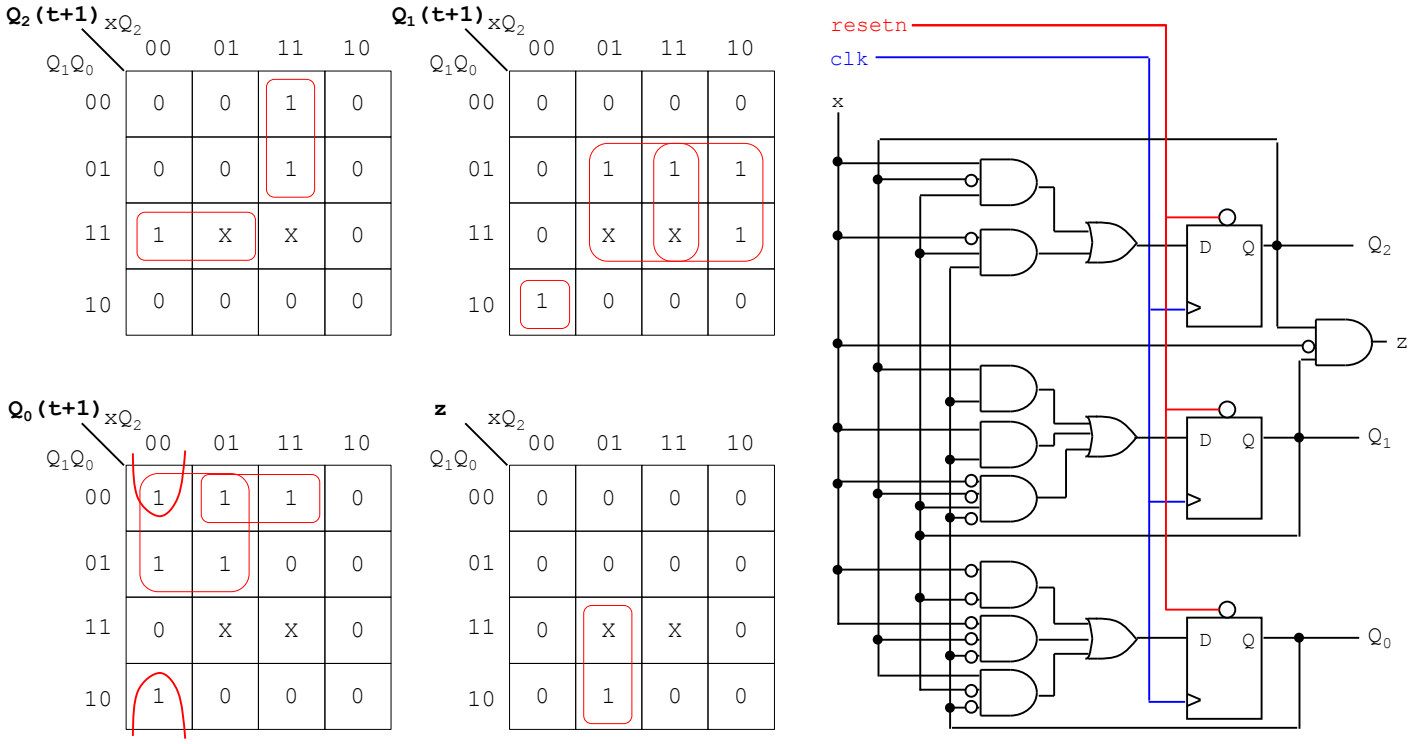
x	PRESENT STATE	NEXT STATE	z
0	S1	S2	0
0	S2	S2	0
0	S3	S4	0
0	S4	S5	0
0	S5	S2	0
0	S6	S4	0
0	S7	S1	1
1	S1	S1	0
1	S2	S3	0
1	S3	S1	0
1	S4	S3	0
1	S5	S6	0
1	S6	S7	0
1	S7	S1	0

	PRESENT STATE	NEXTSTATE	
x	$Q_2Q_1Q_0(t)$	$Q_2Q_1Q_0(t+1)$	z
0	0 0 0	0 0 1	0
0	0 0 1	0 0 1	0
0	0 1 0	0 1 1	0
0	0 1 1	1 0 0	0
0	1 0 0	0 0 1	0
0	1 0 1	0 1 1	0
0	1 1 0	0 0 0	1
0	1 1 1	X X X	X
1	0 0 0	0 0 0	0
1	0 0 1	0 1 0	0
1	0 1 0	0 0 0	0
1	0 1 1	0 1 0	0
1	1 0 0	1 0 1	0
1	1 0 1	1 1 0	0
1	1 1 0	0 0 0	0
1	1 1 1	X X X	X

This is a Mealy FSM. The output 'z' depends on the input as well as on the present state.

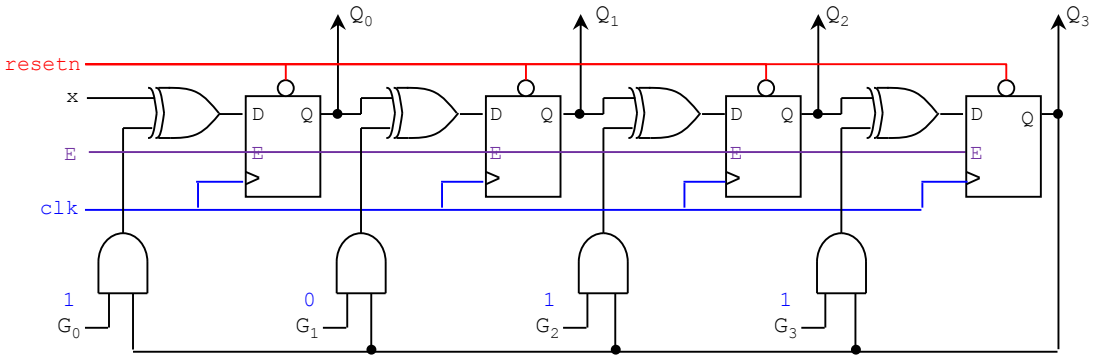
- *Excitation equations, minimization, and circuit implementation:*

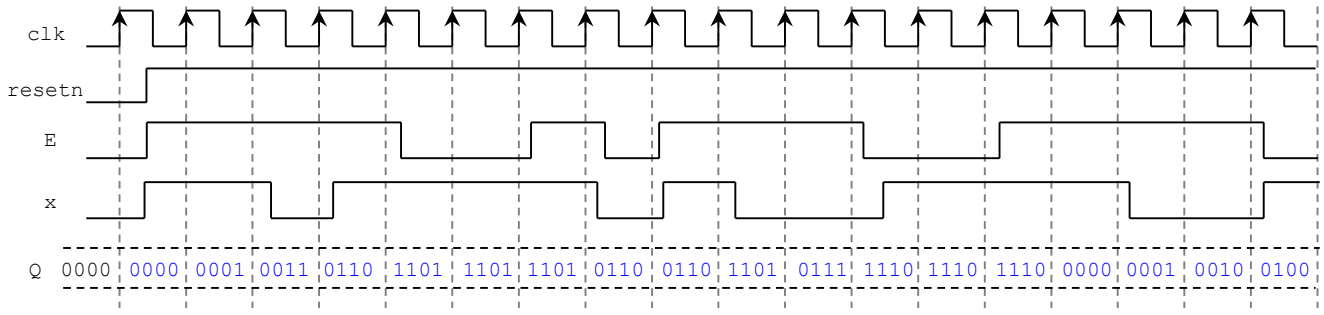
$Q_2(t+1) \leftarrow xQ_2\overline{Q_1} + \bar{x}Q_1Q_0$
$Q_1(t+1) \leftarrow Q_2Q_0 + xQ_0 + \bar{x}\overline{Q_2}Q_1\overline{Q_0}$
$Q_0(t+1) \leftarrow \bar{x}\overline{Q_1} + Q_2\overline{Q_1}\,\overline{Q_0} + \bar{x}\overline{Q_2}\,\overline{Q_0}$
$z = \bar{x}Q_2Q_1$



PROBLEM 2 (15 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1101$, $Q = Q_3Q_2Q_1Q_0$





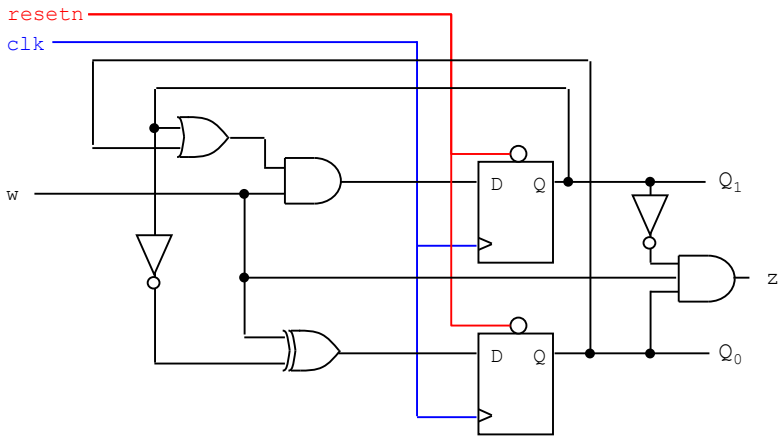
PROBLEM 3 (12 PTS)

- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following FSM.

  w: input, z: output, Q_1Q_0: state.

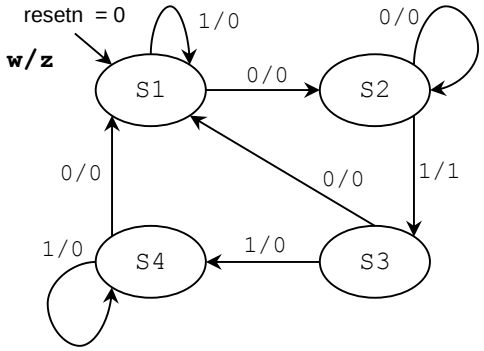
  $Q_1(t+1) \leftarrow (Q_1 + Q_0)w$
  $Q_0(t+1) \leftarrow \overline{Q_1 \oplus w}$
  $z = w\overline{Q_1}Q_0$

  State Assignment:
  S1: Q=00 S2: Q=01
  S3: Q=10 S4: Q=11



PRESENT STATE			NEXTSTATE		
w	Q_1	Q_0 (t)	Q_1Q_0 (t+1)		z
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	1	1	0

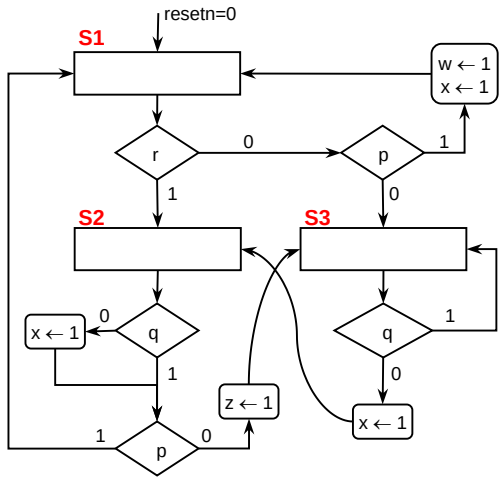
w	PRESENT STATE	NEXT STATE	z
0	S1	S2	0
0	S2	S2	0
0	S3	S1	0
0	S4	S1	0
1	S1	S1	0
1	S2	S3	1
1	S3	S4	0
1	S4	S4	0



PROBLEM 4 (17 PTS)

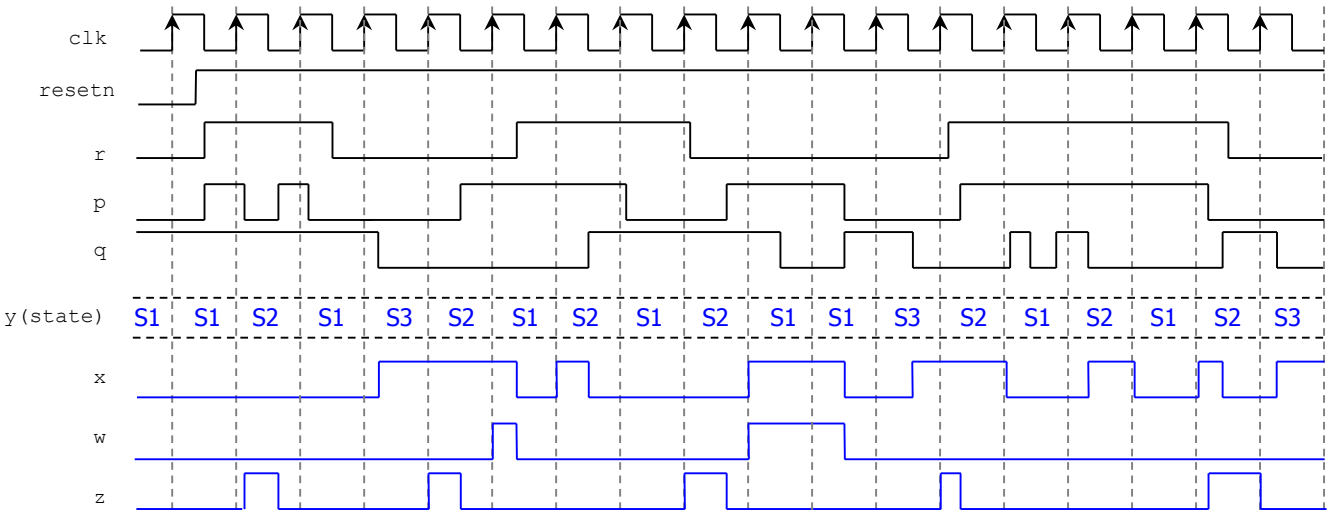
- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```



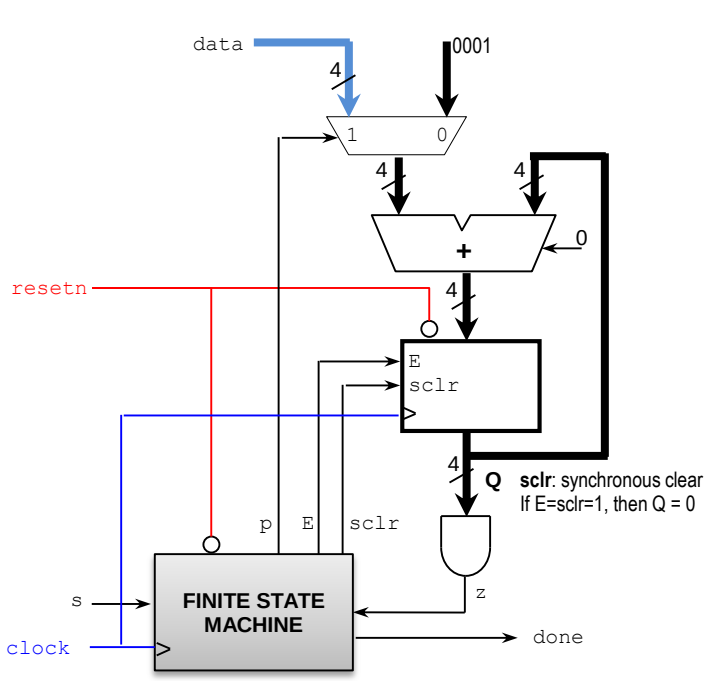

```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, r, p, q)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if r = '1' then
               y <= S2;
            else
               if p = '1' then y <= S1; else y <= S3; end if;
            end if;

          when S2 =>
            if p = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if q = '1' then y <= S3; else y <= S2; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, r, p, q)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if r = '0' then
                       if p = '1' then
                          w <= '1'; x <= '1';
                       end if;
                    end if;

         when S2 => if q = '0' then x <= '1'; end if;
                    if p = '0' then z <= '1'; end if;

         when S3 => if q = '0' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```

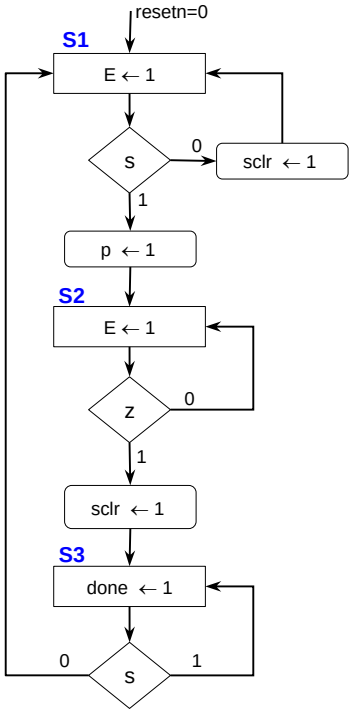
This is a Mealy FSM. The outputs 'x,w,z' depend on the input as well as on the present state.

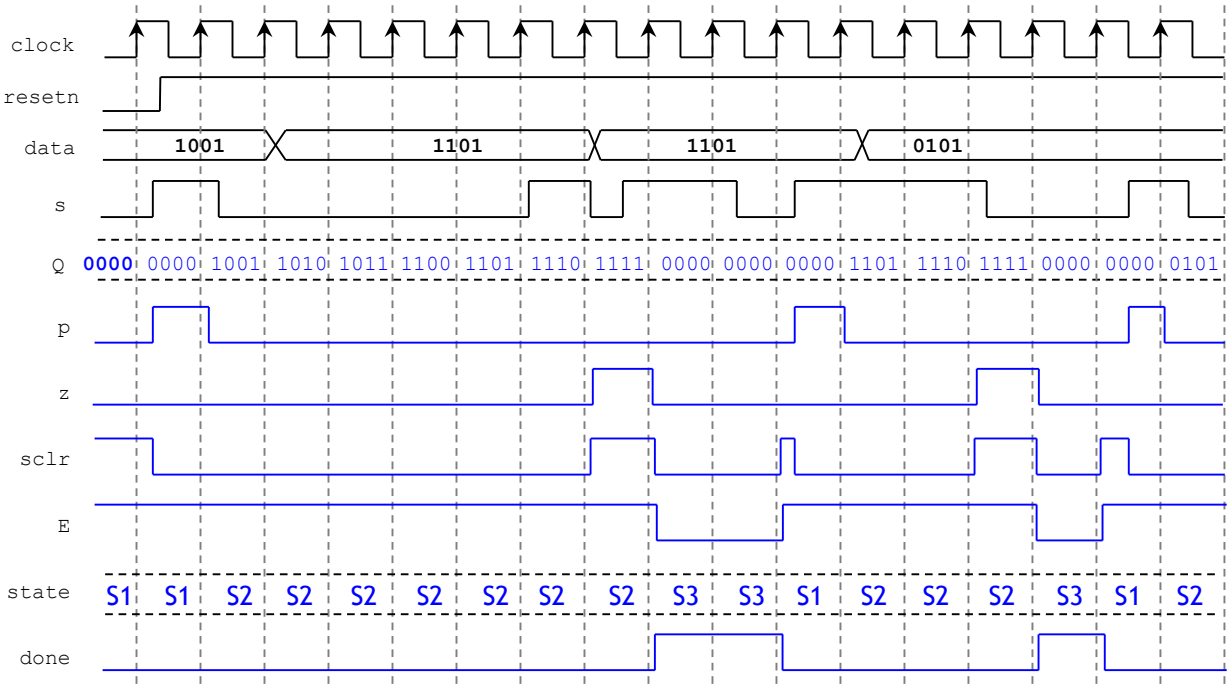


PROBLEM 5 (18 PTS)

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.







PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than three pages, single-spaced, 2 columns). This report should contain the current status of the project. You **MUST** use the provided template (`Final Project - Report Template.docx`).